Chrontel

CH7034B

Advanced Datasheet

CH7034B HDTV/VGA/LVDS Encoder

FEATURES

- Supports multiple output display formats – including Component YPrPb(HDTV), LVDS and analog RGB (VGA)
- Three 10-bit high speed DACs
- HDTV output support up to 1080p
- Analog RGB (VGA) support up to 1920x1080 resolution
- Single channel LVDS 18-bit transmitter supports input resolution up to 1366x768
- Support scaled and bypassed video streams output from VGA/HDTV and LVDS interfaces simultaneously
- Supports panel protection, power sequencing and backlight on/off. PWM is available for controlling LCD brightness
- TV/Monitor connection detect capability. DACs can be switched off through programming internal registers
- On-chip SDRAM frame buffer to support frame rate conversion.
- Programmable adaptive de-flickering filter
- Supports 8/12/16/18/24-bit parallel interface inputs for either RGB format or YCbCr format (ITU-R 656 or ITU-R 601). 80/86 MPU interface and DE only mode are also supported.
- Wide range of input resolutions support for up to 1366x768 (i.e. 640x480 720x480, 720x576, 800x600, 1024x600, 1024x768, 1280x800, and etc.)
- Image display rotation support at 90/180/270 degree or flipped in horizontal/vertical position
- Pixel-level color enhancement for brightness, contrast, hue and saturation adjustment for HDTV
- Horizontal/vertical position adjusted through serial port programming
- Pixel clock input frequency support for up to 165 MHz
- Flexible crystal or oscillator clock input frequency (2.3MHz – 64MHz)
- IO Supply Voltages from 1.2V to 3.3V and SPC/SPD Supply Voltages from 1.8V to 3.3V.
- Programmable power management
- Device fully programmable through serial port or can automatically load firmware from Chrontel Boot ROM (CH9904)
- Offered in a 88-pin QFN package

GENERAL DESCRIPTIONS

Chrontel CH7034B is specifically designed for a portable system that requires connections to LCD display, High Definition Television (HDTV) or RGB (VGA) monitor. With its advanced video encoder, flexible scaling engine and easy-to-configure video interface, the CH7034B satisfies manufactures' product display requirements and reduces their costs of development and time-to-market.

The CH7034B provides analog RGB and YPrPb outputs that allow a system to display high definition media content to HDTV/RGB monitors. The device is compliant with EIA770-3 and SMPTE 274M/293M /296M standards and supports HDTV resolution up to 1080p. The 3 high-performance, 10-bit DACs can be used for either HDTV display or VGA output. The CH7034B has the ability to generate composite syncs if required by the RGB monitor.

To support portable computer with LCD display, the CH7034B has incorporated an one-channel, 18-bit output LVDS transmitter. On-chip dithering function is available to convert 24-bit color to 18-bit color LCD panels. Two popular LVDS standards, the OpenLDI and the VESA SPWG are supported by the CH7034B LVDS driver. The preferred standard and its display timing can be configured through devices' registers when system is powered on.

The CH7034B is equipped with panel protection mechanism to switch off the LCD instantly if input data is missing or unstable. The panel on/off sequences and backlight control can be configured through programming internal registers. In addition, a built-in PWM function can be used to achieve digital dimming for LCD panel.

The CH7034B converts a wide range of input formats to HDTV/VGA outputs and LVDS display. RGB data format such as 16-bit 5:6:5, 18-bit 6:6:6 or 24-bit 8:8:8 enters through the device's 24-bit bus. In YCrCb format, either 24-bit 4:4:4 data or 16-bit 4:2:2 is supported by the CH7034B's color space converter. The device's video capture block also has an option to support 80/86 MPU interface. The input video signal can be either interlaced or non-interlaced data formats.

With its embedded high speed SDRAM, the CH7034B can help manufactures design their products to achieve simultaneous LVDS and HDTV/VGA display. Thanks to the sophisticated scaler, the input LCD data with low resolution or reduced-frame rate can be covert to high

APPLICATION

- Mobile Internet Devices
- Smartbook / Electronic Book
- Tablet Device
- Portable DVD Players
- Docking Station

quality HDTV or VGA display without extra loading on the processor. Also, by taking the advantage of the framebuffer, the scaler can perform other image manipulations including resizing and rotation.

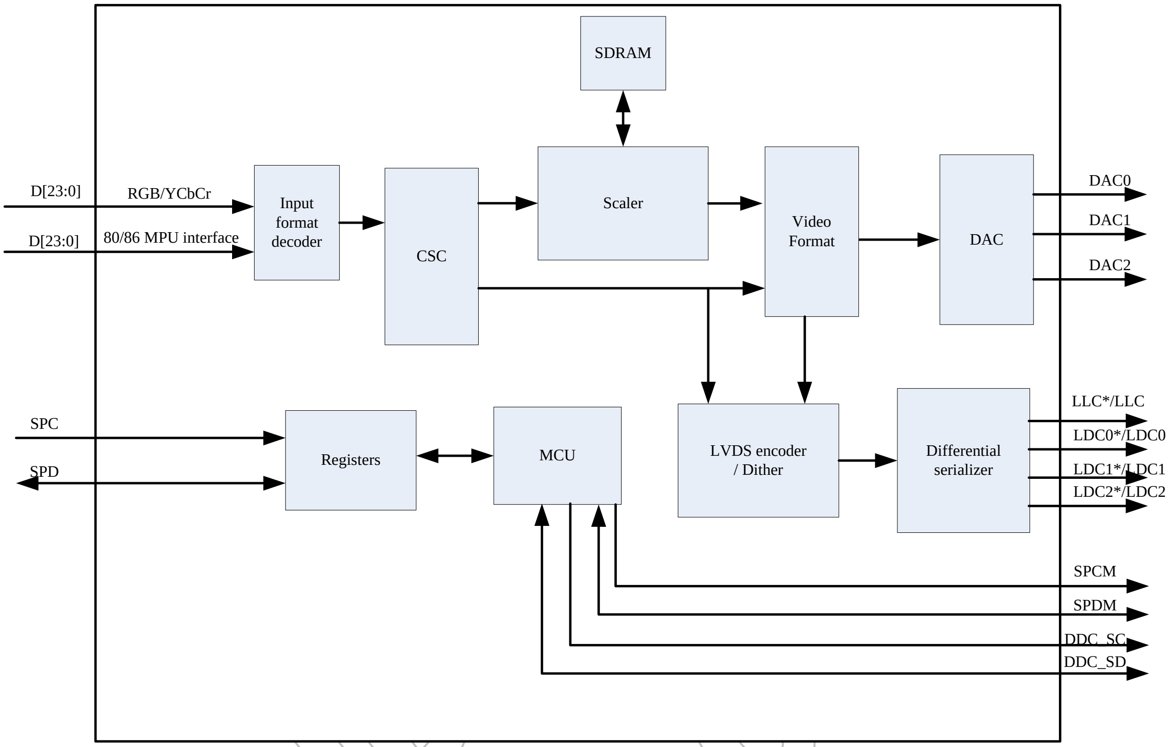
SDRAM
D[23:0]
RGB/YCbCr
D[23:0]
80/86 MPU interface
Input format decoder
CSC
Scaler
Video Format
DAC
DAC0
DAC1
DAC2
SPC
SPD
Registers
MCU
LVDS encoder / Dither
Differential serializer
LLC*/LLC
LDC0*/LDC0
LDC1*/LDC1
LDC2*/LDC2
SPCM
SPDM
DDC_SC
DDC_SD

Figure 1: Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

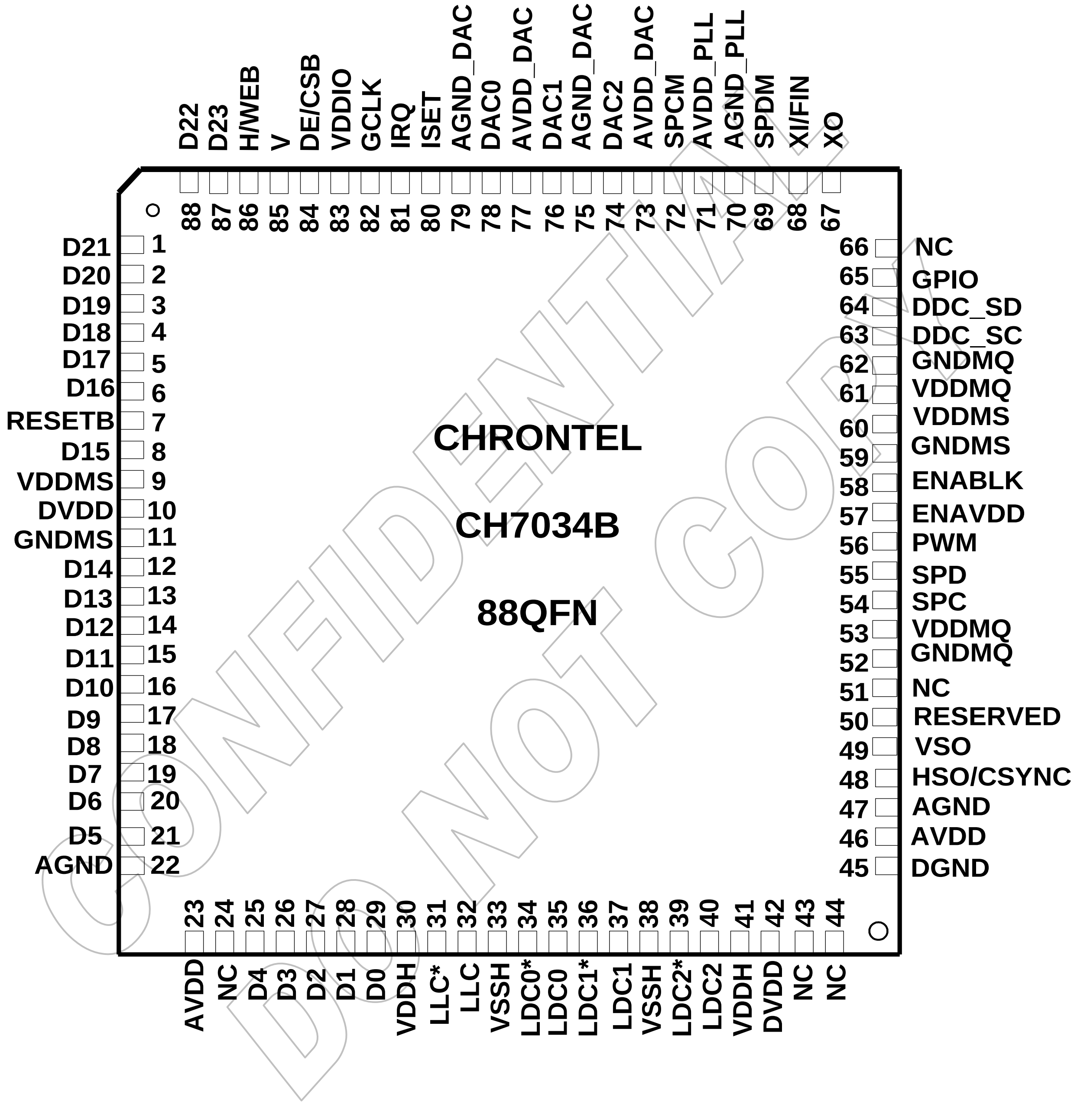
D22 88
D23 87
H/WEB 86
V 85
DE/CSB 84
VDDIO 83
GCLK 82
IRQ 81
ISET 80
AGND_DAC 79
DAC0 78
AVDD_DAC 77
DAC1 76
AGND_DAC 75
DAC2 74
AVDD_DAC 73
SPCM 72
AVDD_PLL 71
AGND_PLL 70
SPDM 69
XI/FIN 68
XO 67
D21 1
D20 2
D19 3
D18 4
D17 5
D16 6
RESETB 7
D15 8
VDDMS 9
DVDD 10
GNDMS 11
D14 12
D13 13
D12 14
D11 15
D10 16
D9 17
D8 18
D7 19
D6 20
D5 21
AGND 22
66 NC
65 GPIO
64 DDC_SD
63 DDC_SC
62 GNDMQ
61 VDDMQ
60 VDDMS
59 GNDMS
58 ENABLK
57 ENAVDD
56 PWM
55 SPD
54 SPC
53 VDDMQ
52 GNDMQ
51 NC
50 RESERVED
49 VSO
48 HSO/CSYNC
47 AGND
46 AVDD
45 DGND
23 AVDD
24 NC
25 D4
26 D3
27 D2
28 D1
29 D0
30 VDDH
31 LLC*
32 LLC
33 VSSH
34 LDC0*
35 LDC0
36 LDC1*
37 LDC1
38 VSSH
39 LDC2*
40 LDC2
41 VDDH
42 DVDD
43 NC
44 NC
CHRONTEL
CH7034B
88QFN

Figure 2: 88 pin QFN Package (Top View)

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
1~6,8, 12~21, 25~29, 87~88,	In	D[23:0]	**Data Input** These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. All the unused Data input pins should be pulled low with 10 KΩ resistors or shorted to Ground directly.
7	In	RESETB	**Reset Input** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
31,32	Out	LLC*,LLC[1]	**LVDS Clock Outputs** These pins provide the differential clock output for the LVDS.
34,35	Out	LDC0*,LDC0[1]	**LVDS Data Channel 0 Outputs** These pins provide the LVDS differential outputs for data channel 0.
36,37	Out	LDC1*,LDC1[1]	**LVDS Data Channel 1 Outputs** These pins provide the LVDS differential outputs for data channel 1.
39,40	Out	LDC2*,LDC2[1]	**LVDS Data Channel 2 Outputs** These pins provide the LVDS differential outputs for data channel 2.
48	Out	HSO/CSYNC	**Horizontal sync signal output** The amplitude of this pin is from 0 to AVDD. It also functions as a Composite sync output
49	Out	VSO	**Vertical sync signal output** The amplitude of this pin is from 0 to AVDD.
50	N/A	Reserved	**Reserved** This pin should be left open or pulled low with a 10 KΩ resistor in the application.
54	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required.
55	In/out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required.
56	Out	PWM	**Backlight brightness adjustment**
57	Out	ENAVDD	**Panel Power Enable** Enable LCD panel VDD
58	Out	ENABLK	**Back Light Enable** Enable back light of LCD panel
63	Out	DDC_SC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.
64	In/out	DDC_SD	**Routed Serial Port Data to DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused
65	In/ out	GPIO	**General Purpose Input Output**
68	In	XI/FIN	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
69	In/Out	SPDM	**Routed Serial Port Data to CH9904 BOOT ROM**

			This pin functions as the bi-directional data pin of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10K to ground if unused.
72	Out	SPCM	**Routed Serial Port Clock Output to CH9904 BOOT ROM** This pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.
74	Out	DAC2	**YPrPb or Analog RGB output** Full swing is up to 1.3V
76	Out	DAC1	**YPrPb or Analog RGB output** Full swing is up to 1.3V
78	Out	DAC0	**YPrPb or Analog RGB output** Full swing is up to 1.3V
80	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2 KΩ, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
81	Output	IRQ	**Programmed Interrupt output.**
82	In	GCLK	**External Clock Inputs** The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
84	In	DE/CSB	**Data Input Indicator** When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also a CSB signal input of CPU interface The amplitude will be 0 to VDDIO.
85	In/Out	V	**Vertical Sync Input/Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
86	In/Out	H/WEB	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
24,43,44, 51,66	N/A	NC	**Not Connect** These pins should be left open.
9,60	Power	VDDMS	**SDRAM Power Supply (3.3V)**
59,11	Power	GNDMS	**SDRAM Ground**
10,42	Power	DVDD	**Digital Power Supply (1.8V)**
45	Power	DGND	**Digital Ground**
23,46	Power	AVDD	**Analog Power Supply (3.3V)**
22,47	Power	AGND	**Analog Ground**
30,41	Power	VDDH	**LVDS Power Supply (3.3V)**
33,38	Power	VSSH	**LVDS Ground**
53,61	Power	VDDMQ	**SDRAM output buffer Power Supply (3.3V)**
52,62	Power	GNDMQ	**SDRAM output buffer Ground**
71	Power	AVDD_PLL	**PLL Power Supply (1.8V)**
70	Power	AGND_PLL	**PLL Ground**

77,73	Power	AVDD_DAC	**DAC Power Supply (3.3V)**
75,79	Power	AGND_DAC	**DAC Ground**
83	Power	VDDIO	**IO Power Supply (1.2-3.3V)**

Notes:

The clock/data order and the polarity of the 4 output channels are programmable.

2.0 FUNCTIONAL DESCRIPTION

2.1 Video Input

2.1.1 Overview

Five distinct methods of transferring data to the CH7034B are described below.

1. Unitary data, clock input at 1X the pixel rate (SDR mode)
2. Multiplexed data, clock input at 1X of pixel rate (DDR mode)
3. Multiplexed data, clock input at 2X of pixel rate
4. Multiplexed data, clock input at 3X of pixel rate
5. 80/86 MPU interface
6. DE only mode

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7034B is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X or 3X pixel rate the data applied to the CH7034B is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7034B is latched with one edge of the clock .The polarity of the pixel clock can be reversed through serial port control. H sync and V sync can be input individually or embedded into data signal such as BT656 input format.

2.1.2 Input Clock and Data Timing Diagram

Figure 3 to **Figure 7** below shows the timing diagram for input data and clocks. The timing requirements are given in later section.

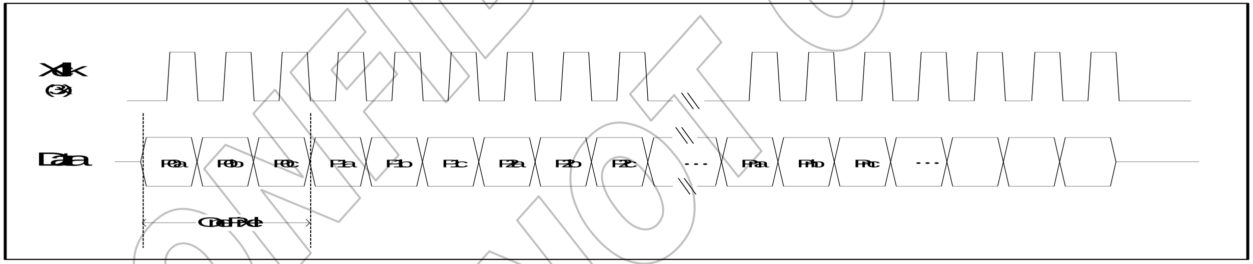

Figure 3: Clock and Data Input Timing in 3x Multiplexed Mode

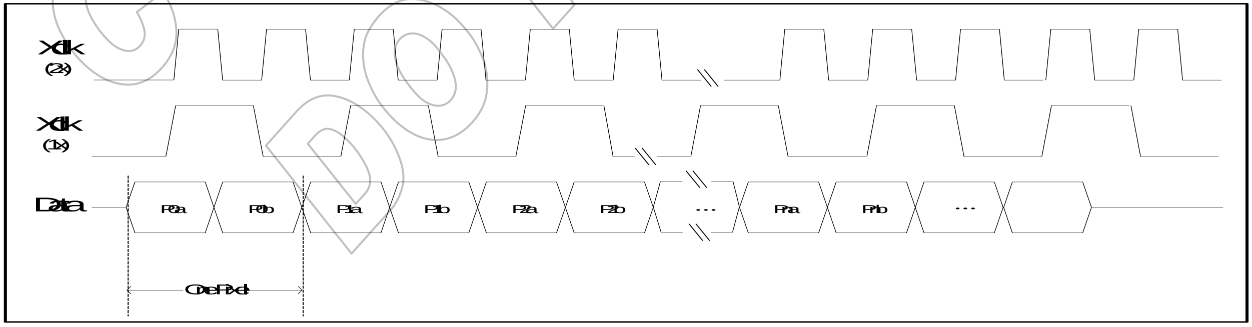

Figure 4: SDR and DDR Input Data Formats

(Note: In **Figure 4**, the first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method.)

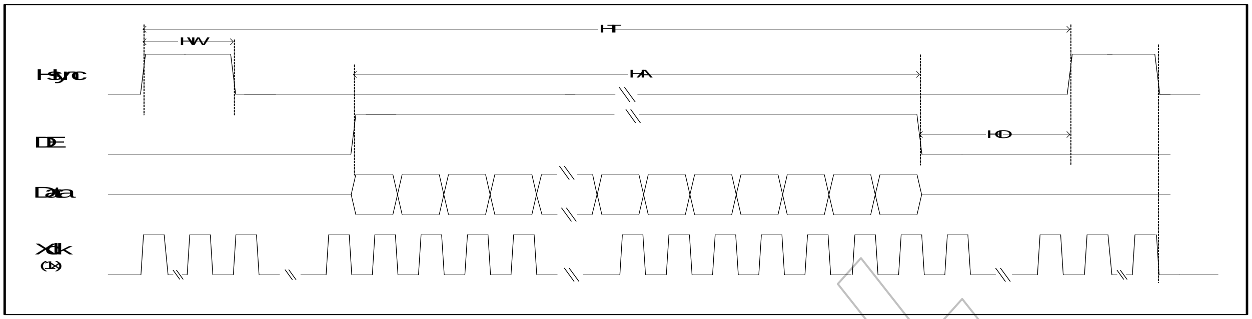

Figure 5: Horizontal Input Timing

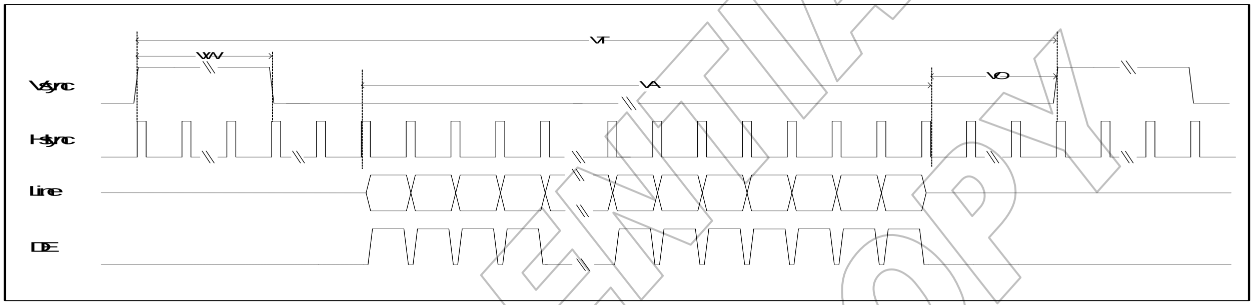

Figure 6: Vertical Input Timing

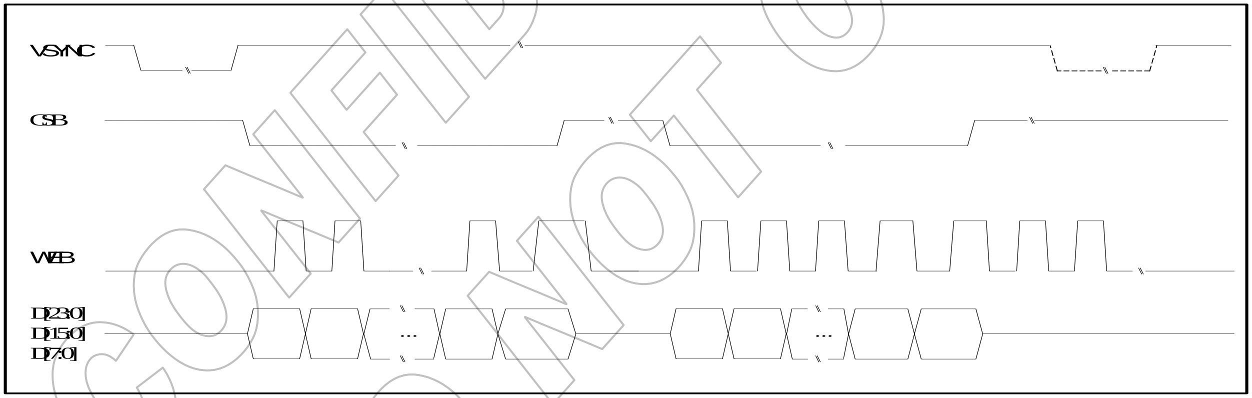

Figure 7: 80/86 MPU Interface Timing

(Note: VSYNC pulse of 80/86 MPU interface is not necessary for each input frame, it is required to appear at least one time at any input frame blank period.)

2.1.3 Input data voltage

The voltage level of input pins D [23:0], H/WEB, V, DE/CSB are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit **DIFFEN** is high, the input is pseudo differential mode that uses a reference voltage (VREF) to compare with input voltage and decide input logic value. The VREF value can be 80%, 70%, 60% and 50% of VDDIO value, referring to **VRTM [1:0]**. The pseudo differential mode can accept the wide range of the input voltage level from 1.2v to 3.3v, while the CMOS mode can accept 1.8v to 3.3v input voltage.

2.1.4 Input data format

The following table indicates the supported input data format by CH7034B.

Table 2: **Input data format**

MULTI		IDF	D [23:16]	D [15:8]	D [7:0]
0		0	R [7:0]	G [7:0]	B [7:0]
		1	2'b00,R [5:0]	2'b00,G [5:0]	2'b00,B [5:0]
		2	3'b000,R [4:0]	2'b00,G [5:0]	3'b000,B [4:0]
		3	3'b000,R [4:0]	3'b000,G [4:0]	3'b000,B [4:0]
		4	R [7:3], G [7:5]	R [2:0], G [1], G [4:2], B [7]	B [6:3], G [0], B [2:0]
		5	8'h00	Y [7:0]	C [7:0]
		6	4'h0, Y [9:6]	Y [5:0], C [9:8]	C [7:0]
		7	Y [7:0]	Cb [7:0]	Cr [7:0]
		9	6'h00, R [5:4]	R [3:0], G [5:2]	G [1:0], B [5:0]
		10	8'h00	R [4:0], G [5:3]	G [2:0], B [4:0]
		11	8'h00	1'b0, R [4:0], G [4:3]	G [2:0], B [4:0]
1	PA	0		4’h0, R [7:4]	R [3:0], G [7:4]
	PB			4’h0, G [3:0]	B [7:0]
	PA	1		7’h00, R [5]	R [4:0], G [5,3]
	PB			7’h00, G [2]	G [1:0], B [5:0]
	PA	2			R [4:0], G [5,3]
	PB				G [2:0], B [4:0]
	PA	3			1’b0,R [4:0], G [4,3]
	PB				G [2:0], B [4:0]
	PA	4		4’h0, R [7:4]	R [3], G [7:5], R [2:0], G [1]
	PB			4’h0, G [4:2], B [7]	B [6:3], G [0], B [2:0]
	PA	5			Y [7:0]
	PB				C [7:0]
	PA	6		6’h00, Y [9:8]	Y [7:0]
	PB			6’h00, C [9:8]	C [7:0]
	PA	7		4’h0, Y [7:4]	Y [3:0], Cb [7:4]
	PB			4’h0, Cb [3:0]	Cr [7:0]
2	PA	0			R [7:0]
	PB				G [7:0]
	PC				B [7:0]
	PA	7			Y [7:0]
	PB				Cb [7:0]
	PC				Cr [7:0]

(PA, PB, PC represent the parts of one pixel data)

IDF [3:0] describes the major input data format that CH7034B accepts. They are:
IDF = 0: 888 RGB input
IDF = 1: 666 RGB input
IDF = 2: 565 RGB input
IDF = 3: 555 RGB input
IDF = 4: special RGB input
IDF = 5: 8-bit YCbCr4: 2: 2 input
IDF = 6: 10-bit YCbCr4: 2: 2 input
IDF = 7: 8-bit YCbCr4: 4: 4 input
IDF = 9: Consecutive aligned 666 RGB input
IDF = 10: Consecutive aligned 565 RGB input
IDF = 11: Consecutive aligned 555 RGB input

Table 2 above describes the 24-bit input data format under unitary mode. For multiplexed input, input data need to be de-multiplexed to unitary input first then this table can be applied. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCbCr formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.: PA and PB) will contains a complete pixel. (3X input has the similar feature)

When the input is a YCbCr data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0, Y0, Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connection error and correct it automatically.

2.2 DAC Output

2.2.1 TV Output

This chip support the following TV output formats:

Table 3: Supported HDTV standards

Standards		Field/Frame Rate(Hz)	Total	Active	Clock(MHz)	Scan Type
480/60p	SMPTE293M EIA770.2A	60/1.001	858x525 or 1716x525	720x480	27 or 54	Progressive
576/50p	ITU-R BT1358	50	864x625 or 1728x625	720x576	27 or 54	Progressive
720/60p	SMPTE296M	60 or 60/1.001	1650x750	1280x720	74.25 or 74.176	Progressive
720/50p	SMPTE296M	50	1980x750	1280x720	74.25	Progressive
1080/60i	SMPTE274M	60 or 60/1.001	2200x1125	1920x1080	74.25 or 74.176	Interlaced
1080/50i	SMPTE274M	50	2640x1125	1920x1080	74.25	Interlaced
1080/50i	SMPTE295M	50	2376x1250	1920x1080	74.25	Interlaced
1080/60p	SMPTE274M	60 or 60/1.001	2200x1125	1920x1080	148.5	Progressive

2.2.2 VGA Output

The CH7034B supports analog RGB output through video DACs. Typically used resolution is 800x600, 1024x768, 1280x800, 1280x1024 and so on. Vertical sync and horizontal sync signal can be provided. Composite sync output is also supported. The type of composite sync can be programmed through register map.

2.2.3 DAC output Configuration

Table 5 below lists the DAC output configurations of CH7034B:

Table 4: Video DAC Configurations for CH7034B

DACSP[2:0] (page1 R75[2:0])	DAC0	DAC1	DAC2
0	Y(R)	Pb(G)	Pr(B)
1	Y(R)	Pr(B)	Pb(G)
2	Pb(G)	Y(R)	Pr(B)
3	Pb(G)	Pr(B)	Y(R)
4	Pr(B)	Y(R)	Pb(G)
5	Pr(B)	Pb(G)	Y(R)

2.2.4 DAC single/double termination

The DAC output of the CH7034B can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. Refer to the description of register bit **SEL_R**(page2 R1A[5])

2.2.5 TV connection detect

The chip can detect the TV connection by setting register SPPSNS. It can detect whether DAC are connected, short to ground or not connected.

2.2.6 Picture enhancement

CH7034B has the capability of vertical and horizontal output picture position adjustment. For HDTV output it can provide brightness, contrast, hue, saturation adjustment and text enhancement functions. For analog RGB output, brightness, contrast adjustment and text enhancement are available.

The CH7034B also supports vertical or horizontal flip and rotation (90, 180 and 270 degree) functions.

For 90,270 degree rotate output mode, the input resolution support up to 720x1440(RGB-565), if true color (RGB-888) support up to 720x720.

2.3 LVDS Output

In this chip, the LVDS output supported 18-bit single pixel format defined by OpenLDI and SPWG. The 18-bit single pixel format represents a pixel as three 6-bit values, one each for the intensity of red, green and blue.

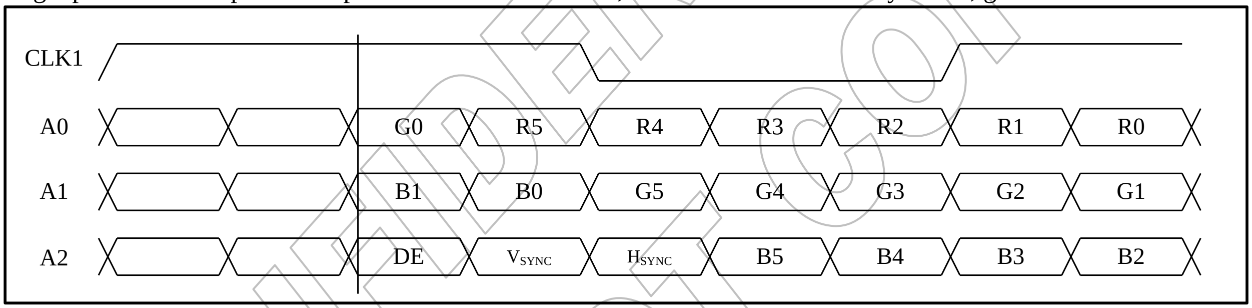

Figure 8: 18 bits single pixel format

There are 3 serial data lines(A0 through A2) and one clock line(CLK1) in LVDS interface. The serial data stream on each signal line shall be at a bit rate that is seven times the pixel rate.

2.3.1 Power Sequencing

The chip conforms to SPWG's requirements on power sequencing. The timing specification shown in **Figure 9** is a superset of the requirements dictated by the SPWG specification. The timing parameters can be programmed to different values via the opcode commands to suit requirements by different panels.

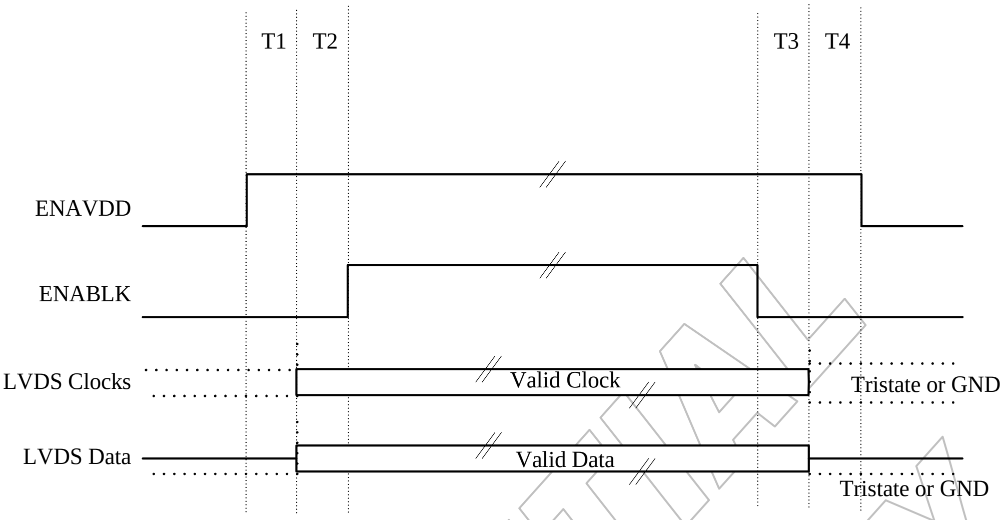

Figure 9: Power Sequencing

Table 5: Power Sequencing

Timing Parameter	Range	Increment
T1	1-50 ms	1ms
T2	200-1023 ms	1ms
T3	200-1023 ms	1ms
T4	1-50 ms	1ms

2.4 Testing Functions and Power Down Mode

2.4.1 Test Pattern Select

Setting TSTP [3:0] of 7Fh on the first page of register map can select different video patterns that go through datapath, according to the following table. TEST (bit4 of 7Fh on the first page) has to be 1 to enable test mode. TSYNC is to select which sync will be used internally generated sync or external input sync.

Table 6: Test Pattern Selection

TSTP [3:0]	Test pattern
0	External data
1	White
2	Vertical ramp
3	Horizontal ramp
4	Color bar
7	Production test pattern
11	Sine wave output for DAC test
13	Ramp output for DAC test

2.4.2 SDRAM Power Down

SDRAM has two kinds of power down modes. One is power down mode, the other is deep power down mode. For power down mode, all data contents will be held in the bank. For deep power down mode, a command is required to issued. There is a bit called MEMPD in register map. It can be used to enable the deep power mode. During deep power mode, all the data in memory banks will be lost, and the SDRAM leakage current is less than 1µA. **A very important thing required to be noted here is that not all the SDRAM parts support either power down or deep power down mode**. In these cases, even CH7034B enters into power down, the leakage current is still large (> 100µA). In deep power down mode, the current consumption of SDRAM is less than 10µA. (This leakage current is primarily derived from the SDRAM die.)

3.0 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All 1.8V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		2.5 5.0	V
	Input voltage of all digital pins	GND – 0.5		VDDIO+0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature (Commercial / Automotive Grade 4)	0		70	°C
T_{AMB}	Ambient operating temperature (Industrial / Automotive Grade 3)	-40		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS1}	Vapor phase soldering (5 seconds)			260	°C
T_{VPS2}	Vapor phase soldering (11 seconds)			245	°C
T_{VPS3}	Vapor phase soldering (60 seconds)			225	°C

Note:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power Supply Voltages by more than ± 0.5V can induce permanent damage.
3. The digital input voltage will follow the I/O Supply Voltage (VDDIO), the I/O Supply Voltage range is from 1.2V to 3.3V.

3.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDDMQ/ VDDMS	SDRAM interface supply	3.135	3.3	3.5	V
GNDMQ/ GNDMS	SDRAM interface ground		0		V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
DGND	Digital ground		0		V
AVDD	Analog power supply	3.135	3.3	3.5	V
AGND	Analog ground		0		
VDDH	LVDS output driver power supply	3.135	3.3	3.5	V
VSSH	LVDS output driver ground		0		V
AVDD_PLL	PLLs power supply	1.71	1.8	1.89	V
AGND_PLL	PLLs ground		0		V
AVDD_DAC	DAC Power Supply Voltage	2.5	3.3	3.5	V
AGND_DAC	DAC ground		0		V
VDDIO	Data I/O Supply Voltage	1.14		3.5	V
VDD18	Generic for all 1.8V supplies[1]	1.71	1.8	1.89	V

VDD33	Generic for all 3.3V supplies[1]	3.135	3.3	3.5	V

Note:
VDD18 and VDD33 don’t include VDDMQ and VDDMS

3.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD18=1.8V± 5%, VDD33 =2.5V – 3.5V)

Symbol	Description	Min	Typ	Max	Units
	Video DAC Resolution	10	10	10	bits
	Full scale output current of each DAC		38		mA
	Video level error of DAC			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		111.8		mA
I_{VDD33}	Total VDD33 supply current (3.3V supplies) (Refer to note)		131		mA
I_{VDDQ}	Memory data interface supply current		0.10		mA
I_{VDD_MEM}	Memory core supply current		15		mA
I_{PD}	Total Power Down Current[1]		<20		uA

Notes:
1. If the chip is not in deep power down mode, the total power down current will be about 6mA. Most of the leakage current is come from the SDRAM.

3.4 Digital Inputs / Outputs DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	serial port data (SPD/SPDM/SPCM) Output Low Voltage	I_{OL} = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.2		VDD33 + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD,SPDM) Input Low Voltage		GND-0.5		0.4	V
V_{SPMIH}	Serial Port (SPDM) Input High Voltage		2.0		VDD33 + 0.5	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{IRQH}	Interrupt pin (IRQ) output high voltage		VDDIO*0.8		VDDIO+0.5	V
V_{IRQL}	Interrupt pin (IRQ) output Low voltage		GND-0.5		0.4	V
V_{DATAIH}	Data I/O (1) High Voltage		VDDIO/2+0.25		VDDIO + 0.5	V
V_{DATAIL}	Data I/O Low Voltage		GND-0.5		VDDIO/2-0.25	V
V_{MISCIH}	Miscellaneous Input High Voltage (2)		VDD33 – 0.5		VDD33 + 0.5	V
V_{MISCIL}	Miscellaneous Input Low Voltage (2)		GND-0.5		0.6	V
V_{SYNCOH}	Miscellaneous Output High Voltage (3)		VDD33 x 0.8			V
V_{SYNCOL}	Miscellaneous Output Low Voltage (3)				0.3	V

I_{MISCPU}	Miscellaneous Input Pull Up Current (2)	$V_{IN} = 0$	0.5		5.0	uA
I_{MISCPD}	Miscellaneous Input Pull Down Current (2)	V_{IN} = VDD33	0.1		1.1	uA

Notes:

1. Applies to D[23:0], GCLK, H, V and DE. VDDIO is the I/O supply, ranging from 1.2V to 3.3V.
2. Applies to RESETB and ATPG.
3. Applies to HSO, VSO,ENABKL,ENAVDD,PWM

3.5 Digital Inputs / Outputs AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$f_{CRYSTAL}$	Input (CRYSTAL) frequency			27		MHz
f_{GCLK}	Input (GCLK) frequency		1.5		165	MHz
DC_{GCLK}	Input (GCLK) Duty Cycle	$T_S + T_H < 1.2$ns	30		70	%
t_{GJIT}	GCLK clock jitter tolerance			10		ns
t_S	Setup Time: D[23:0], H, V and DE to GCLK	GCLK to D[23:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[23:0], H, V and DE to GCLK	D[23:0], H, V, DE = Vref to GCLK	0.5			ns

3.6 LVDS Output Specifications

The LVDS specifications meet the requirements of ANSI/EIA/TIA-644. Refer to figure 10 for definitions of parameters.

(Operating Conditions: T_A = 0°C – 70°C, VDD18 =1.8V ± 5%, VDD33=3.3V± 5%)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$\lvert V_t \rvert$	Steady State Differential Output Magnitude for logic 1	100Ω differential load	247		453	mV
$\lvert V_t{*} \rvert$	Steady State Differential Output Magnitude for logic 0	100Ω differential load	247		453	mV
$\lvert V_t \rvert - \lvert V_t{*} \rvert$	Steady State Magnitude of Differential between Logic 1 and 0 Outputs	100Ω differential load			50	mV
$\lvert V_{OS} \rvert$	Steady State Magnitude of Offset Voltage for Logic 1	Measured at centertap of two 50Ω resistors connected between outputs	1.125		1.375	V
$\lvert V_{OS}{*} \rvert$	Steady State Magnitude of Offset Voltage for Logic 0	Measured at centertap of two 50Ω resistors connected between outputs	1.125		1.375	V
$\lvert Vos \rvert - \lvert Vos{*} \rvert$	Steady State Magnitude of Offset Difference between Logic States	Measured at centertap of two 50Ω resistors connected between outputs			50	mV
f_{LLC}	LVDS Output Clock Frequency		25		165	MHz

Symbol	Description	Test Condition	Min	Typ	Max	Unit
t_{UI}[1]	LVDS data unit time interval	25MHz < f_{LLC}<165MHz	0.86		5.7	ns
t_R	LVDS data rise time	100Ω and 5pF differential load				
	t_{UI} > 5ns				0.3*t_{UI}	ns
	1.526ns<t_{UI}<5ns	20%->80% Vswing	0.26		1.5	ns
t_F	LVDS data fall time	100Ω and 5pF differential load				
	t_{UI} > 5ns				0.3*t_{UI}	ns
	0.86ns<t_{UI}<5ns	80%->20% Vswing	0.26		1.5	ns
Vring	Voltage ringing after transition	100Ω nd 5pF differential load			20% Vswing	

3.7 LVDS Output Timing

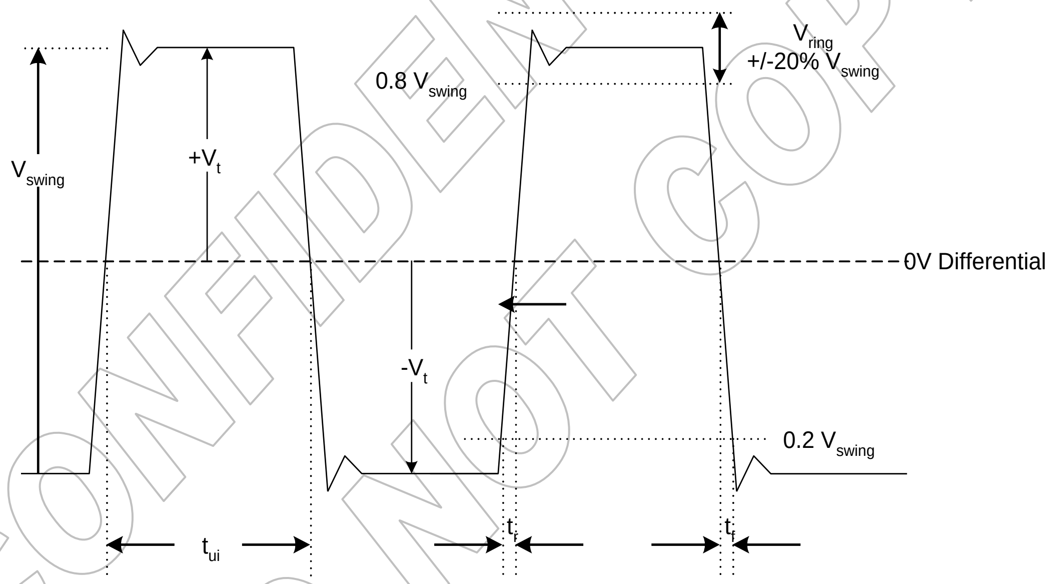

Figure 10: AC Timing for LVDS Outputs

Table 7: AC Timing for LVDS Outputs

Symbol	Parameter	Min	Typ	Max
$\|V_t\|$	Steady State Differential Output Magnitude	Refer to section 4.6		
V_{SWING}	Voltage Difference between the two Steady State Values of Output	$\|V_t\| + \|V_t{}^*\|$		
t_{Ui}	Unit time interval	Refer to section 4.6		
t_r	Rise time	Refer to section 4.6		
t_f	Fall time	Refer to section 4.6		

4.0 PACKAGE DIMENSIONS

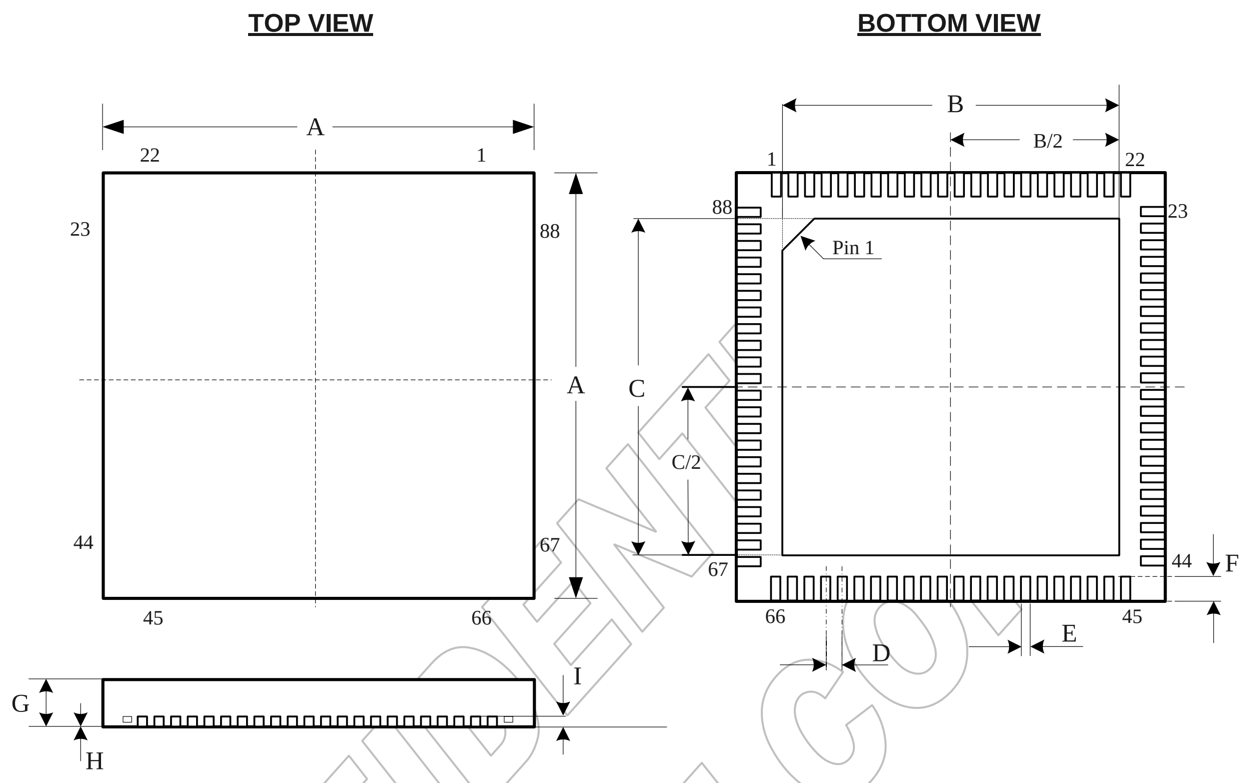
TOP VIEW
BOTTOM VIEW
A
22
1
23
88
A
44
67
45
66
G
H
I
B
B/2
1
22
88
23
Pin 1
C
C/2
67
44
F
66
45
E
D

Figure 11: 88 Pin QFN Package (10 x 10 mm)

Table of Dimensions

No. of Leads		**SYMBOL**								
88 (10 X 10 mm)		**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**
Milli-meters	**MIN**	**9.90**	**6.65**	**6.65**	**0.30**	**0.15**	**0.40**	**0.80**	**0**	**0.20**
	NOM	**10.00**	**6.75**	**6.75**	**0.40**	**0.20**	**0.50**	**0.85**	**-**	
	MAX	**10.10**	**6.85**	**6.85**	**0.50**	**0.25**	**0.60**	**0.90**	**0.05**	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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5.0 REVISION HISTORY

Rev. #	Date	Section	Description
1.0	03/04/2011	All	Official release.
1.1	07/06/2011	Features 1.1, 1.2 2..2.6	Update some descriptions. Update pin description Update descriptions, picture enhancement
1.2	09/15/2011	2.3.1	Update LVDS power on sequence
1.21	10/10/2012	3.1	Update the absolute maximum ratings
1.22	07/23/2013	4.0	Update the package dimension
1.23	11/19/2013	4.0	Update the package dimension
1.3	04/11/2016	4.0	Update the package dimension

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7034B-BF	88QFN, Lead-free	Commercial : 0 to 70°C	168/Tray
CH7034B-BFI	88QFN, Lead-free	Industrial : -40 to 85°C	168/Tray

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